Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 12, 18, 38, 39, 41, 43, 44, 46, and 51-60. Please amend claim 42, as follows:

Listing of Claims:

1-4. (Cancelled)

5. (Previously amended) The memory hub of claim 35 wherein the non-volatile memory is further coupled to the link interface.

6-23. (Cancelled)

24. (Previously presented) The processor-based system of claim 47 wherein the plurality of memory devices comprises synchronous dynamic random access memory devices.

25-34. (Cancelled)

35. (Previously presented) A memory hub for a hub-based memory sub-system, comprising:

a link interface for receiving memory access requests;

an electrically programmable non-volatile memory having memory module configuration information stored therein;

a first configuration path coupled to the link interface and the electrically programmable non-volatile memory, the first configuration path configured to provide the link interface access to the electrically programmable non-volatile memory;

a second configuration path coupled to the electrically programmable non-volatile memory and configured to provide access to the electrically programmable non-volatile memory;

a local serial bus coupled to the electrically programmable non-volatile memory and configured to provide a host system access to the electrically programmable non-volatile memory; and

a memory controller coupled to the link interface and further coupled to the electrically programmable non-volatile memory through the second configuration path, the memory controller having registers into which the memory configuration information is loaded, the memory controller operable to access the electrically programmable non-volatile memory through the second configuration path and further operable to output memory requests in response to receiving memory access requests from the link interface and in accordance with the memory configuration information loaded in the registers.

36. (Previously presented) The memory hub of claim 35 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

37-41. (Cancelled)

42. (Currently amended) The memory sub-system of claim 35 [[38]] wherein the memory ~~module~~ configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

43-46. (Cancelled)

47. (Previously presented) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

an input/output channel coupled to the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, comprising:

a link interface for receiving memory access requests from the system controller;

an electrically programmable non-volatile memory having memory module configuration information for the plurality of memory devices stored therein;

a first configuration path coupled to the link interface and the electrically programmable non-volatile memory, the first configuration path configured to provide the link interface access to the electrically programmable non-volatile memory;

a second configuration path coupled to the electrically programmable non-volatile memory and configured to provide access to the electrically programmable non-volatile memory;

a local serial bus coupled to the electrically programmable non-volatile memory and configured to provide a host system access to the electrically programmable non-volatile memory; and

a memory controller coupled to the link interface and further coupled to the electrically programmable non-volatile memory through the second configuration path, the memory controller operable to access the electrically programmable non-volatile memory through the second configuration path and further operable to output memory requests to the plurality of memory devices in response to receiving memory access requests from the link interface and in accordance with the memory configuration information stored by the electrically programmable non-volatile memory.

48. (Previously presented) The processor-based system of claim 47 wherein the electrically programmable non-volatile memory comprises an embedded array of electrically erasable programmable read-only memory.

49. (Cancelled)

50. (Previously presented) The processor-based system of claim 47 wherein the memory configuration information comprises at least one of timing information for the plurality of memory devices of the memory module, memory module configuration data, memory device type, and manufacturer data.

51-60. (Cancelled)